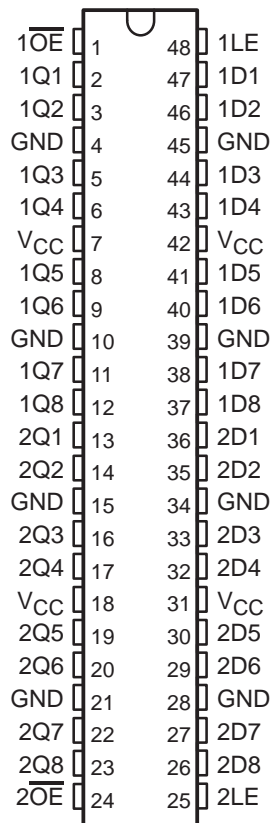


SN54AHCT16373, SN74AHCT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS336H – MARCH 1996 – REVISED JANUARY 2000

- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16373 . . . WD PACKAGE
SN74AHCT16373 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16373 devices are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT16373 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AHCT16373 is characterized for operation from -40°C to 85°C.



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 **TEXAS
INSTRUMENTS**

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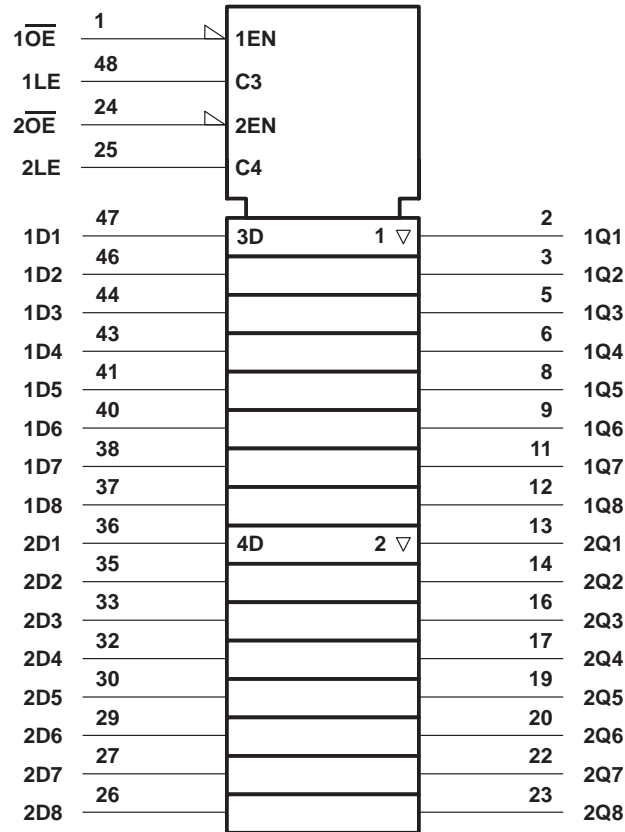
SN54AHCT16373, SN74AHCT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS336H – MARCH 1996 – REVISED JANUARY 2000

FUNCTION TABLE
(each 8-bit latch)

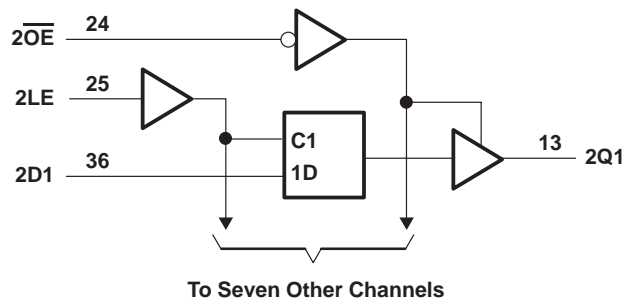
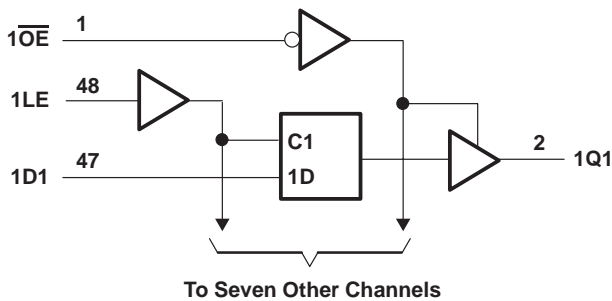
INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54AHCT16373, SN74AHCT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS336H – MARCH 1996 – REVISED JANUARY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through each V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGW package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

	SN54AHCT16373		SN74AHCT16373		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	5.5	0	5.5	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–8		–8	mA
I_{OL} Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20		20	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHCT16373, SN74AHCT16373
16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCLS336H – MARCH 1996 – REVISED JANUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT16373		SN74AHCT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1			0.1	V	
	I _{OL} = 8 mA				0.36		0.44	0.44		
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	40	μA	
ΔI _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10			10	pF	
C _o	V _O = V _{CC} or GND	5 V		4.5					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHCT16373		SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	6.5		6.5		6.5		ns
t _{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t _h	Hold time, data after LE↓	3.5		3.5		3.5		ns



SN54AHCT16373, SN74AHCT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS336H – MARCH 1996 – REVISED JANUARY 2000

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT16373		SN74AHCT16373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	C _L = 15 pF	5.1*	8.5*		1*	9.5*	1	9.5	ns
t _{PHL}				5.1*	8.5*	1*	9.5*	1	9.5		
t _{PLH}	LE	Q	C _L = 15 pF	5*	8.5*		1*	9.5*	1	9.5	ns
t _{PHL}				5*	8.5*	1*	9.5*	1	9.5		
t _{PZH}	\overline{OE}	Q	C _L = 15 pF	5*	9.5*		1*	10.5*	1	10.5	ns
t _{PZL}				5*	9.5*	1*	10.5*	1	10.5		
t _{PHZ}	\overline{OE}	Q	C _L = 15 pF	6*	10.2*		1*	11*	1	11	ns
t _{PLZ}				6.8*	10.2*	1*	11*	1	11		
t _{PLH}	D	Q	C _L = 50 pF	5.9	9.5		1	10.5	1	10.5	ns
t _{PHL}				5.9	9.5	1	10.5	1	10.5		
t _{PLH}	LE	Q	C _L = 50 pF	6.4	9.5		1	10.5	1	10.5	ns
t _{PHL}				5.9	9.5	1	10.5	1	10.5		
t _{PZH}	\overline{OE}	Q	C _L = 50 pF	6	10.5		1	11.5	1	11.5	ns
t _{PZL}				6	10.5	1	11.5	1	11.5		
t _{PHZ}	\overline{OE}	Q	C _L = 50 pF	6.8	11.2		1	12	1	12	ns
t _{PLZ}				7.8	11.2	1	12	1	12		
t _{sk(o)} [†]			C _L = 50 pF			1**			1	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT16373			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.32	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.1	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.7		V
V _{IH(D)}	High-level dynamic input voltage		2		V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load, f = 1 MHz	22	pF

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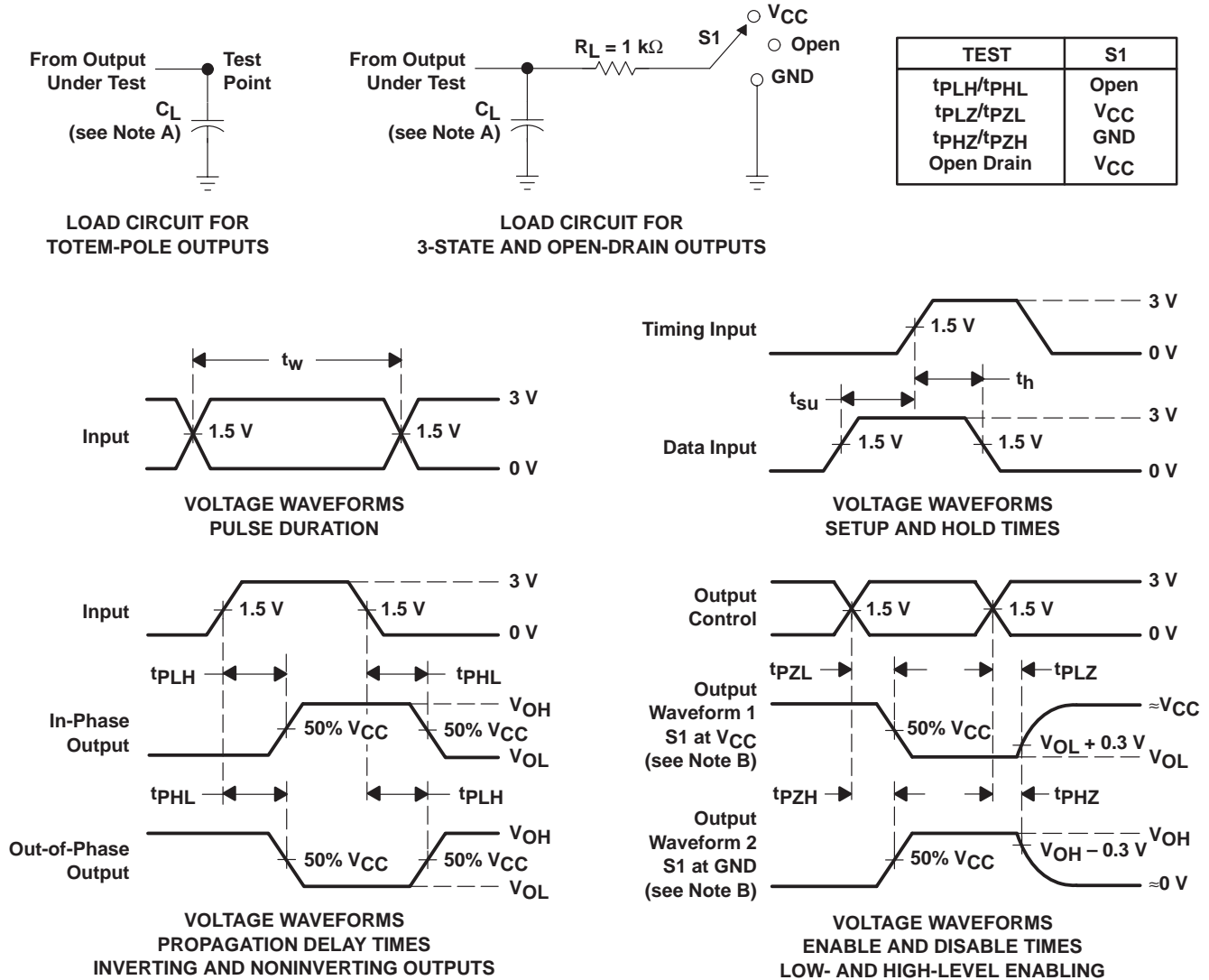


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SN54AHCT16373, SN74AHCT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AHCT16373DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16373DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16373DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16373DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16373DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16373DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16373DGVV	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16373DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16373DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16373DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

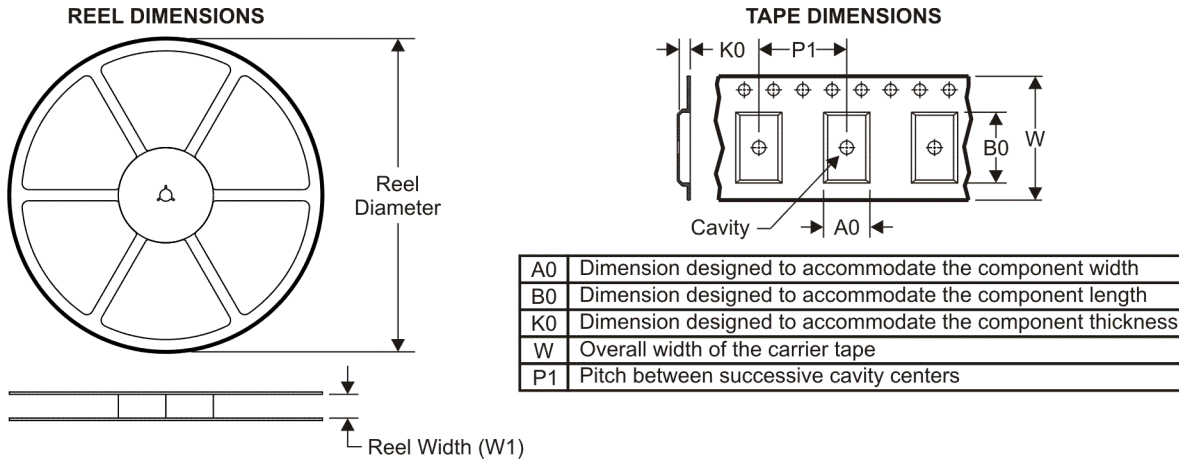
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

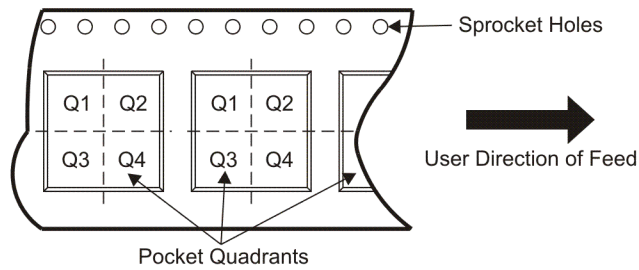
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TAPE AND REEL INFORMATION



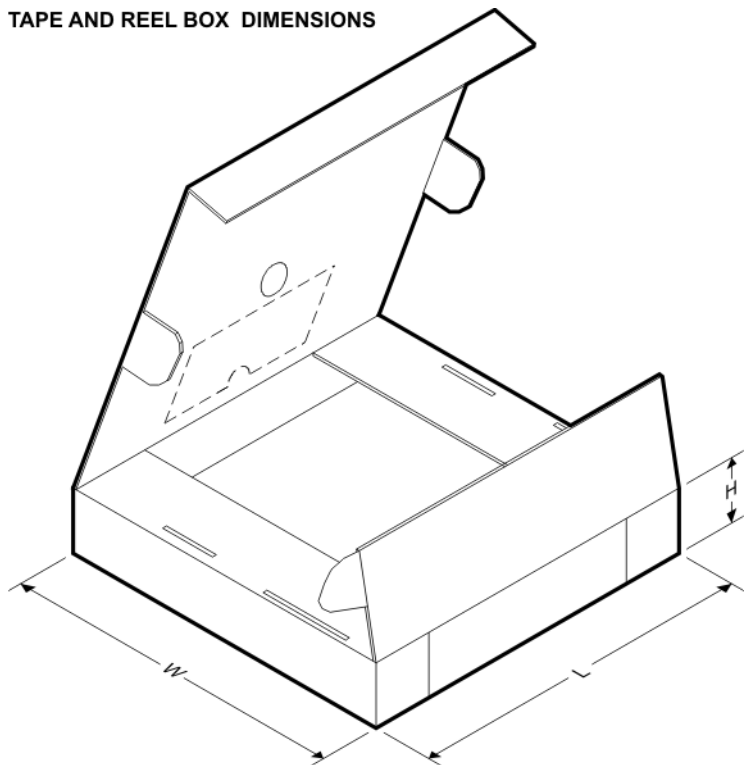
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT16373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AHCT16373DGVR	TVSOP	DGV	48	2000	330.0	24.4	6.8	10.1	1.6	12.0	24.0	Q1
SN74AHCT16373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



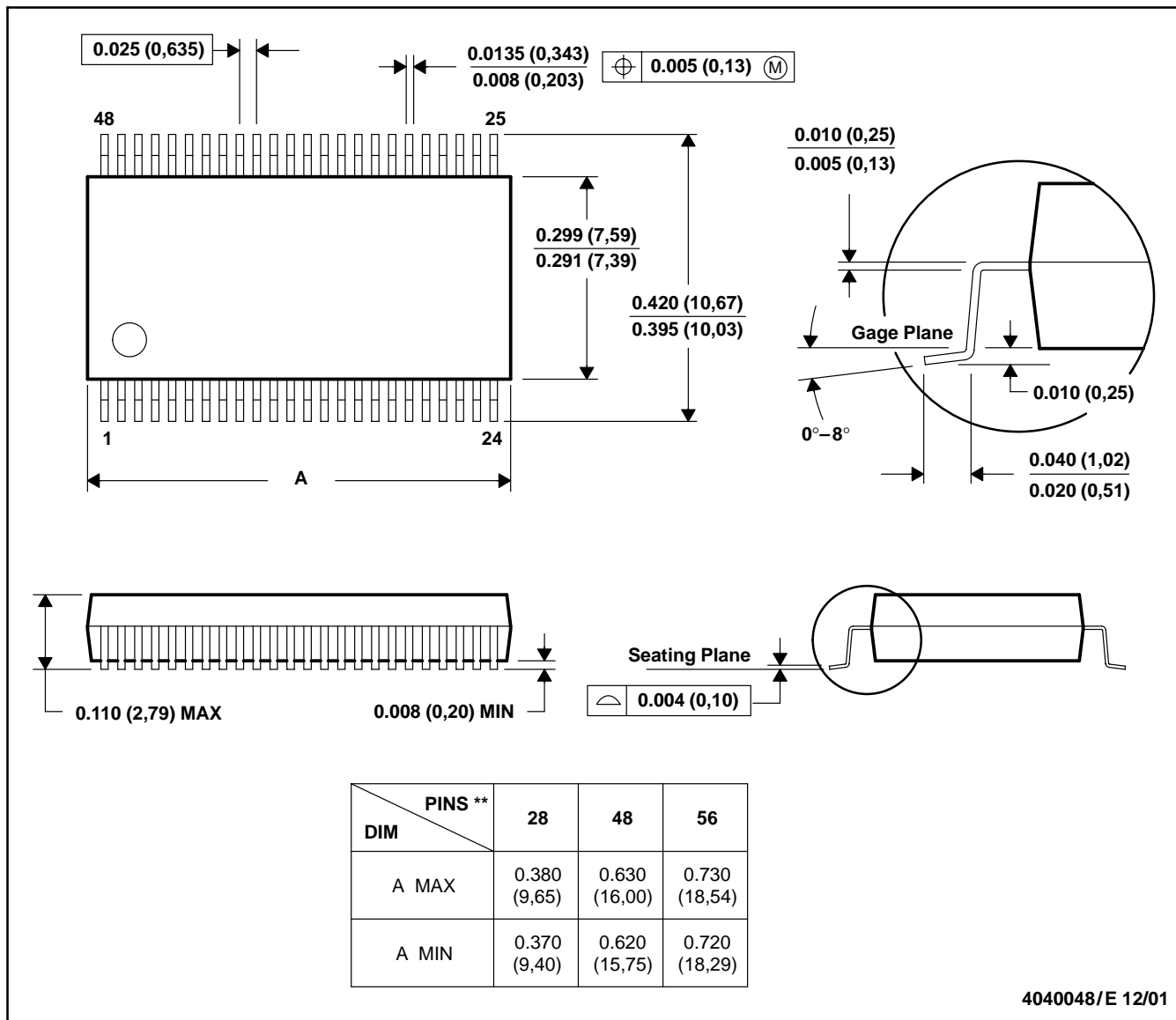
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT16373DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74AHCT16373DGVR	TVSOP	DGV	48	2000	346.0	346.0	41.0
SN74AHCT16373DLR	SSOP	DL	48	1000	346.0	346.0	49.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

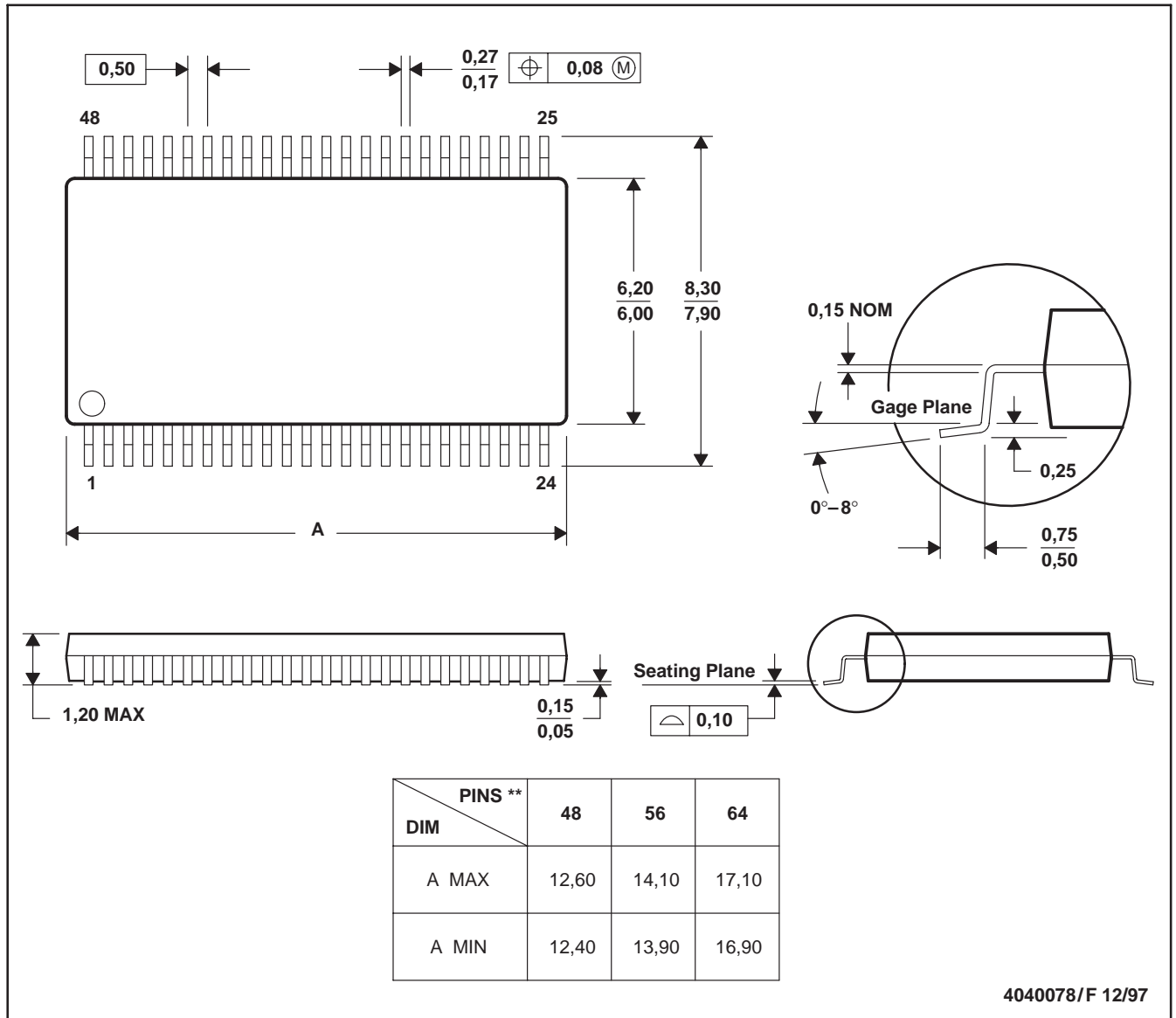


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

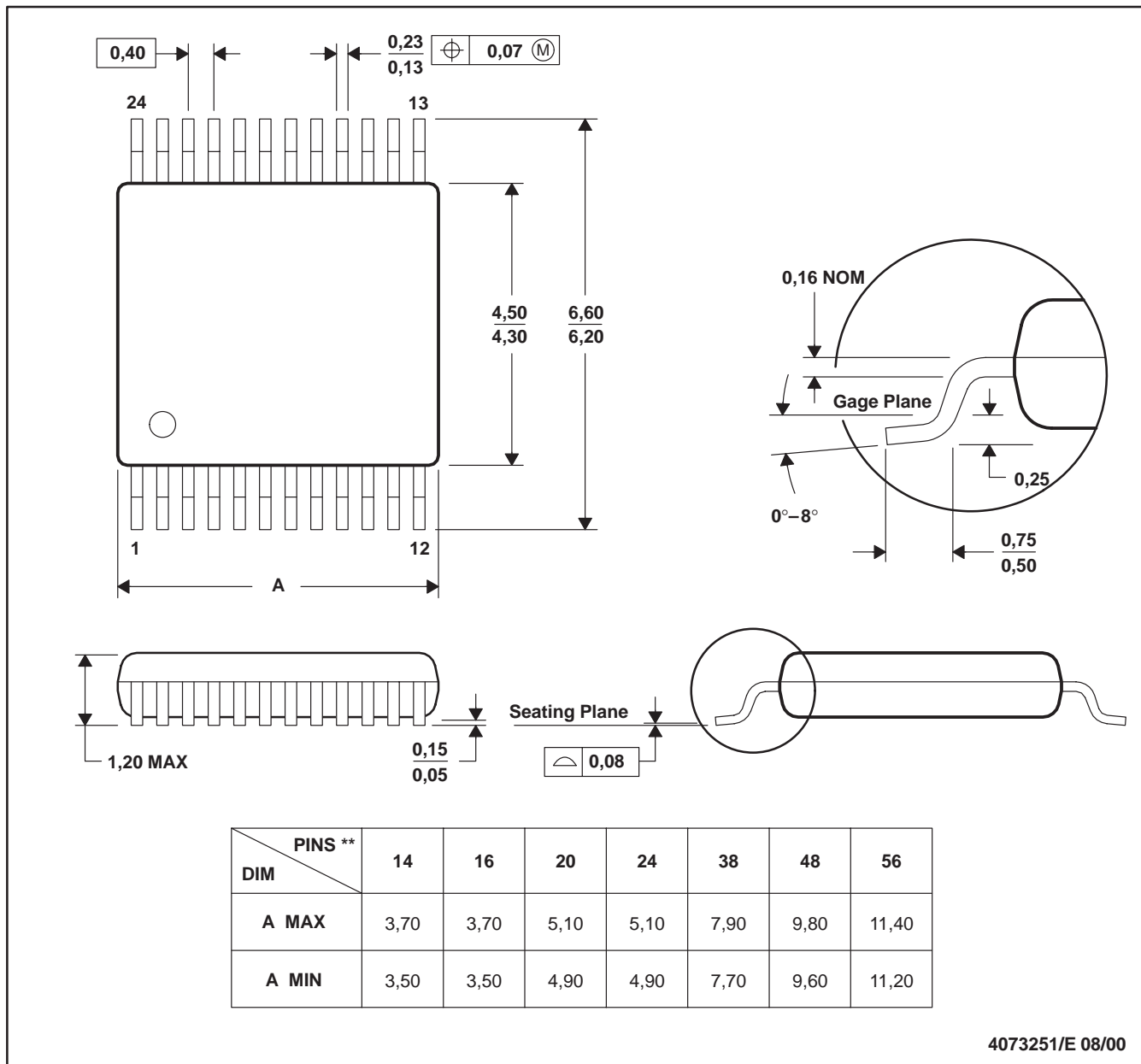


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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